Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the present application:

Listing of the Claims:

1-13. (Canceled)

14. (Currently amended) A resistor pattern for an integrated circuit memory device having a capacitor, comprising:

an integrated circuit substrate;

a low resistive layer formed on the integrated circuit substrate, the low resistive layer defining an upper capacitor electrode of the capacitor and defining a low resistive layer of the resistor pattern in a region of the integrated circuit substrate displaced from the upper capacitor electrode;

an insulating layer formed on the upper capacitor electrode and the low resistive layer of the resistor pattern; and

a high resistive layer formed on the insulating layer, wherein the low resistive layer, the insulating layer and the high resistive layer together define ~~defining~~ the resistor pattern in the region of the integrated circuit substrate displaced from the upper capacitor electrode.

15. (Currently amended) The resistor pattern of Claim 14 wherein the low resistive layer comprises a material having a specific resistance of less than about one ~~at least a~~ hundred μΩcm ~~μΩ•cm~~.

16. (Original) The resistor pattern of Claim 15 wherein the low resistive layer comprises at least one of Ru, Pt, RuO_2, Ir, IrO_2, W, Al, Cu, TiN, TaN, and/or WN.

17. (Original) The resistor pattern of Claim 14 wherein the insulating layer comprises at least one of SiO_2, Ta_2O_5, Al_2O_3, and/or Si_3N_4.

18. (Currently amended) The resistor pattern of Claim 14 wherein the high resistive layer has a specific resistance of at least [[a]] one hundred μΩcm ~~μΩ•cm~~.

19. (Currently amended) The resistor pattern of Claim 18 wherein the high resistive layer has a specific resistance of at least [[a]] one thousand μΩcm ~~μΩ•cm~~.

20. (Original) The resistor pattern of Claim 18 wherein the high resistive layer comprises a doped polysilicon layer.

21. (Original) The resistor pattern of Claim 14 further comprising, a TiN layer formed between the low resistive layer and the insulating layer.

22-32. (Canceled)

33. (New) An integrated circuit device, comprising:

a low resistive layer on an integrated circuit substrate having a first portion defining an upper electrode of a capacitor of the integrated circuit device and a second portion, separated from the first portion, in a region of the integrated circuit device displaced from the upper electrode;

an insulating layer on the low resistive layer opposite the integrated circuit substrate; and

a high resistive layer, having a specific resistance higher than the low resistive layer and of at least about one hundred μΩcm, on the insulating layer opposite the low resistive layer, wherein the second portion of the low resistive layer and the insulating layer and the high resistive layer on the second portion of the low resistive layer define the resistor pattern in the region of the integrated circuit substrate displaced from the upper electrode.

34. (New) The device of Claim 33 wherein the integrated circuit device is an integrated circuit memory device including the capacitor and wherein the second portion of the low resistive layer defining the resistor pattern and the upper capacitor electrode are formed of the same material.

35. (New) The device of Claim 34 wherein the low resistive layer comprises at least one of ruthenium (Ru), platinum (Pt), ruthenium oxide (RuO_2), iridium (Ir), iridium oxide (IrO_2), tungsten (W), aluminum (Al), copper (Cu), titanium nitride (TiN), tantalum

nitride (TaN) and/or tungsten nitride (WN) and wherein the high resistive layer comprises a doped polysilicon.

36. (New) The device of Claim 35 wherein the insulating layer comprises at least one of SiO_2, Ta_2O_5, Al_2O_3 and/or Si_3N_4.

37. (New) The device of Claim 34 further comprising at least one of a source and/or a drain in a cell region of the integrated circuit memory device between the the resistor pattern and the capacitor.

38. (New) The device of Claim 34 further comprising:

a first metal contact extending to the upper capacitor electrode; and

a second metal contact, having a depth different from a depth of the first metal contact, extending to the high resistive layer of the resistor pattern.

39. (New) The device of Claim 34 further comprising a titanium nitride (TiN) layer between the low resistive layer and the insulating layer.